-- 14. In an address multiplex dynamic RAM having a plurality of memory cells and a plurality of operational modes, a circuit arrangement comprising:

a first external terminal for receiving a row address strobe signal;

a second external terminal for receiving a column address strobe signal;

a third external terminal for receiving a write enable signal;

a fourth external terminal for receiving a designating signal designating one of said operational modes;

a first circuit having first, second and third input terminals which are coupled to said first, second and third external terminals, respectively; and

a second circuit having first and second input terminals which are coupled to an output of said first circuit and to said fourth external terminal, respectively,

wherein said first circuit detects levels of said row address strobe signal, said column address strobe signal and said write enable signal, and said second circuit sets said designating signal into a holding circuit in response to said column address strobe signal being at a logic "low" level, said write enable signal being at a logic "low" level and said row address strobe signal being at a logic "low" level.

~~30.~~ 16 In an address multiplex dynamic RAM having a plurality of memory cells and a plurality of operational modes, a circuit arrangement comprising:

a first external terminal for receiving a row address strobe signal;

a second external terminal for receiving a column address strobe signal;

a third external terminal for receiving a write enable signal;

a fourth external terminal for receiving a designating signal designating one of said operational modes;

a detecting circuit having first, second and third input terminals which are coupled to said first, second and third external terminals, respectively; and

a setting circuit having a control terminal and a data input terminal which are coupled to a detection output of said detecting circuit and to said fourth external terminal, respectively;

wherein said detecting circuit detects levels of said row address strobe signal, said column address strobe signal and said write enable signal, and said setting circuit sets said designating signal into a holding circuit in response to said column address strobe signal being at a logic "low" level, said write enable signal being at a logic "low" level and said row address strobe signal being at a logic "low" level. --